Specification

The Field Effect Transistor in Sandwich Configuration having Organic Semiconductors and Manufacturing Process Thereof

FIELD OF THE TECHNOLOGY

The present invention relates to a Field Effect Transistor (to be abbreviated as FET hereinafter) and manufacturing process thereof, more particularly, to a FET having a sandwich structure in which a source electrode and a drain electrode are sandwiched between semiconductors and manufacturing process thereof.

BACKGROUND OF THE TECHNOLOGY

In recent years, the research on organic semiconductor is exceptionally active. The performance of the organic FET is superior to that of the amorphous silicon thin film transistor (a-Si:H TFT). In particular, the mobility of some organic micro-molecule oligomers (e.g. Pentacene, Tetracene, etc.) is over 1 (square centimeter per volt per second) at room temperature. So, the organic FET is potential in such practical applications as flexural integrated circuit (to be abbreviated as IC hereinafter), active matrix display and so on.

The organic FET generally adopts the bottom electrode configuration or the top electrode configuration. W099/40631 disclosed a device with a vertical geometrical configuration. Figure 1 shows the existing three geometrical configurations which were applied to obtain the organic FET, wherein, 1 represents the substrate, 2 represents the gate electrode, 3 represents the insulation layer, 4 represents the active layer and 5 represents the source and drain electrodes.

The devices having a bottom electrode configuration and a vertical configurations, respectively, have the advantage of easy to be integrated and processed. But it is difficult to make the later produced organic semiconductor contact with the source and drain electrodes effectively, so that the performance of the devices having two above configurations is inferior to that of the device having a

top electrode configuration. Because the organic semiconductor materials are sensitive to some chemical solvents generally used in the processing of the inorganic semiconductor devices, there is difficulty in processing the device having a top electrode configuration by the conventional process for processing inorganic semiconductor devices.

The active layer of the existing organic FET is made of the material with the same molecule. US P 5,629,530 disclosed an organic FET having an active layer made of the molecules of the electron donor and receptor together. Because this kind of the semiconductor applies the principle of intermingling P with N to conduct electricity, the performances of switching current ratio and mobility of the FET device with this semiconductor are very poor.

SUMMARY OF THE INVENTION

The objective of this invention is to provide a FET in which an active semiconductor layer contacts with the source and drain electrodes effectively. The FET shall can be easily integrated and processed.

Another objective of this invention is to provide a process for manufacturing the present FET.

To achieve these objectives, according to one aspect of the invention, there is provided a FET comprising:

a substrate (1),

a gate electrode (2) formed on the substrate (1),

a gate insulation layer (3) formed on the substrate (1) and the gate electrode (2),

which is characterized in that, further comprising:

an active layer (4) formed on the gate insulation layer (3) but leaving a part of the gate insulation layer (3) to be exposed,

a source and drain electrodes (5) formed on a part of the gate insulation layer (3) and a part of the active layer (4),

an active layer (6) formed on the exposed part of the gate insulation layer (3),

the active layer (4), the source electrode and the drain electrode (5).

According to another aspect of the present invention, there is provided a process for producing the present FET, comprising:

a. forming a layer of conducting material on a substrate and then forming a gate electrode by the method of photolithography ;

b. forming an insulation layer on the substrate and the gate electrode;

c. Vaporously depositing a semiconductor layer on a part of the insulation layer while leaving the other part of the insulation layer exposed;

d. forming a layer of conducting material on the exposed insulation layer and the semiconductor layer, and forming a source electrode and a drain electrode by the photolithography method or delaminating method;

e. Vaporously depositing or spin-coating a semiconductor layer on the source electrode, the drain electrode, the exposed semiconductor layer and the exposed insulation layer.

Taking full advantage of that the organic semiconductor can be processed under low temperature, the present invention adopts two or more kinds of materials to form the active semiconductor layer, makes the active layer contact with the source/drain electrode more effectively, reduces the threshold voltage of the device, and contacts the semiconductor with the source/drain electrode and the insulation layer tightly.

BRIEF DISCRIPTION OF THE FIGURES

Figure 1a shows an example of the conventional FET having a top electrode geometrical configuration.

Figure 1b shows an example of the conventional FET having a bottom electrode geometrical configuration.

Figure 1c shows an example of the conventional FET having a vertical geometrical configuration.

Figure 2 illustrates the structure of the present sandwiched FET.

Figure 3 illustrates the application procedure of the present sandwiched FET.

Figure 4 shows the output characteristic curve of the present sandwiched FET

in example 1, where the active layer adopts non-holonomic CuPc layer, the composite layer of CuPc and CuPc, the composite layer of NiPc and NiPc, the composite layer of CuPc and NiPc respectively.

Figure 5a shows the output characteristic curve of the present sandwiched FET in example 2, where the active layer adopts the composite layer of CuPc and CuPc, the composite layer of CuPc and NdPc, the single layer of NdPc respectively.

Figure 5b shows the transfer characteristic curve of the present sandwiched FET in example 2, where the active layer adopts the composite layer of CuPc and CuPc, the composite layer of CuPc and NdPc respectively.

Figure 6 shows the output characteristic curve of the present top electrode structural device whose active layer is composed of the eutectic organic semiconductor of CuPc and NiPc.

Herein, "Pc" represents "phthalocyanine" and "Nc" represents "Naphthocyanine".

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention will be described with reference to the accompanying drawings.

Figure 2 illustrates the structure of the present sandwiched FET. The conducting material layer is set on the substrate (1) to form the gate electrode (2). The insulation material is set on the substrate and the gate electrode to form the gate insulation layer (3). The hole semiconductor is set on the gate insulation layer to form part of the active layer (4). The conducting material is set on the hole semiconductor layer and the gate insulation layer to form the source and drain electrode (5). In addition, together with the hole semiconductor, part of the semiconductor (6) is set on the gate insulation layer, the semiconductor layer, the gate of the source electrode and the drain electrode to form the active layer.

According to one example of the present invention, the eutectic and laminate structure of the existing model P type semiconductor CuPc and NiPc is adopted to form a kind of active semiconductor. Compared with a single kind of material, this

active semiconductor's current on/off ratio has no obvious loss, while its threshold voltage has been reduced markedly and its carrier mobility has been greatly improved. The principle is that a semiconductor made of the mixture, eutectic and laminate of several kinds of material have good contact with the surfaces of the source and drain electrodes than the semiconductor made of a single kind of material does.

According to one example of the present invention, the laminate structure of the existing model P type semiconductor CuPc and the resistance material $NdPc_2$ is adopted to form a kind of active semiconductor. Compared with a single kind of material, this active semiconductor's switching current ratio and carrier mobility have been greatly improved, while its threshold voltage has been reduced markedly. The principle is that a semiconductor formed by laminating two kinds of material have good contact with the surfaces of the source and drain electrodes than CuPc does. Meanwhile, the field effect transmission property of CuPc is enhanced by $NdPc_2$.

Figure 6 also shows the output characteristic curve of the CuPc/NiPc eutectic FET. When V_G equals to -30V, the FET's hole carrier mobility is 0.04 $cm^2/V.s$ in the saturation region, and its current on/off ratio is $4x10^5$, and the threshold voltage is -8V.

The organic semiconductor of the present invention is made of the mixture, eutectic and laminate of various molecular materials. Compared with the device made of a single material, the properties of this FET, such as, the mobility, the threshold and the switching current ratio are improved markedly.

Now the present invention will be further illustrated with reference to the following examples.

Example 1:

Copper phthalocyanine (CuPc), zinc phthalocyanine (ZnPc), nickel phthalocyanine (NiPc), cobalt phthalocyanine (CoPc), H_2Pc, TiOPc, VOPc and Pentacene used in this example were commercial products, and they were sublimated and purified before being used.

On the 7059 glass substrate or the flexible plastic substrate 1, a film layer of

metal Ta with about 200 nm in thickness was plated by using the radio frequency (RF) magnetism controlled sputtering method and shaped into the gate electrode 2 by the photolithography method. On the grid electrode, a film layer of Ta_2O_5 with a thickness of about 100 nm was reactively sputterred as the gate insulation layer 3 by the direct current (DC) magnetism controlled sputtering method. Then depositing CuPc using the molecular vapor phase deposition method to prepare the active layer 4 having a thickness of about 20 nm. Subsequently, using Au to prepare the source electrode and the drain electrode 5 with a thickness of about 50 nm. Finally, depositing one selected from a group consisting of CuPc, ZnPc, NiPc, CoPc, H_2Pc, TiOPc, VOPc or Pentacene using the molecular vapor phase deposition method to form the active layer 6 having a thickness of about 30nm.

Figure 4 shows the output characteristic curve of the FET sandwiched with CuPc but having no active layer 6 when V_G is -30V. From it, no obvious field effect was observed.

Figure 4 shows the output characteristic curve of the CuPc/CuPc sandwich FET when V_G is -30V. The FET's hole carrier mobility is 0.01 $cm^2/V.s$ in the saturation region, its threshold voltage is -18V, and its current on/off ratio is $4x10^4$.

Figure 4 also shows the output characteristic curve of the NiPc/NiPc sandwich FET when V_G is -30V. The FET's hole carrier mobility is 0.005 $cm^2/V.s$ in the saturation region, its current on/off ratio is $4x10^4$ and its threshold voltage is -16V when V_G is -30V.

Figure 4 also shows the output characteristic curve of the CuPc/NiPc sandwich FET when V_G is -30V. The FET's hole carrier mobility is 0.01 $cm^2/V.s$ in the saturation region, its current on/off ratio is $4x10^5$ and its threshold voltage is -13.5V when V_G is -30V.

Compared with the CuPc/CuPc sandwich FET and the NiPc/NiPc sandwich FET, the CuPc/NiPc sandwich FET presents no obvious variation in the switching current ratio, but its threshold voltage is obviously reduced. Table 1 lists the performance parameters of the existing organic sandwich FET, in which, the mobility and threshold voltage are determined when V_G equals to -30V.

Table 1

Semiconductor 4	Semiconductor 6	Hole mobility $cm^2/V.s$	Threshold Voltage -V
CuPc	CuPc	0.01	18
NiPc	NiPc	0.005	16
CuPc	NiPc	0.01	13.5
CuPc/NiPc (eutectic)		0.04	8
CuPc	ZnPc	0.006	5
CuPc	CoPc	0.003	11
CuPc	H_2Pc	0.007	17
CuPc	TiOPc	0.009	17
CuPc	VOPc	0.01	15
CuPc	Pentacene	0.01	8

Example 2:

All the twin-Pc metals (e.g. $LaPc_2$, $CePc_2$, $PrPc_2$, $NdPc_2$, $SmPc_2$, $EuPc_2$, $GdPc_2$, $TbPc_2$, $DyPc_2$, $HoPc_2$, $ErPc_2$, $TmPc_2$, $YbPc_2$, $LuPc_2$, YPc_2, $ZrPc_2$, $HfPc_2$, $SnPc_2$), H_2Nc, CoNc, CuNc, ZnNc and NiNc used in the present example were synthesized by the methods discussed in the following references: (1) J. Jiang, R. C. W. Liu, T. C. W. Mack, T. D. W. Chan, D. K. P. Ng, Polyhedron, 1997, 16, 515; (2) W. Liu, J. Jiang, D. Du, D. P. Arnold, Aust. J. Chem., 2000, 53, 131; (3) R. Polley, M. Hanack, J. Org. Chem., 1995, 60, 8278; (4) M. hanack, R. Polley, S. Knecht, U. Schlick, Inorg. Chem., 1995, 34, 3621; (5) M. L. Kaplan, A. J. Lovinger, W. D. Reents, jun, P. H. Schmidt, Mol. Cryst. Liq. Cryst., 1984, 112, 345. They were sublimated and purified before being used.

On the 7059 glass substrate or the flexible plastic substrate 1, a film layer of metal Ta with about 200 nm in thickness was plated by using the radio frequency (RF) magnetism controlled sputtering method and shaped into the gate electrode 2 by the

photolithography method. On the gate electrode, a film layer of Ta_2O_5 with a thickness of about 100 nm was reactively sputterred as the gate insulation layer 3 by the direct current (DC) magnetism controlled sputtering method. Then depositing CuPc using the molecular vapor phase deposition method to prepare the active layer 4 having a thickness of about 20 nm. Subsequently, using Au to prepare the source electrode and the drain electrode 5 with a thickness of about 50 nm by the photolithography technology. Finally, depositing one selected from a group consisting of twin-Pc metals ($LaPc_2$, $CePc_2$, $PrPc_2$, $NdPc_2$, $SmPc_2$, $EuPc_2$, $GdPc_2$, $TbPc_2$, $DyPc_2$, $HoPc_2$, $ErPc_2$, $TmPc_2$, $YbPc_2$, $LuPc_2$, YPc_2, $ZrPc_2$, $HfPc_2$, $SnPc_2$), H_2Nc, CoNc, CuNc, ZnNc and NiNc using the molecular vapor phase deposition method to form the active layer 6 having a thickness of about 30nm.

Figure 5 shows the transfer characteristic curves of the NdNc top electrode FET and the NdNc sandwich FET. From it, we can see that the NdNc top electrode FET presents no field effect, while the NdNc sandwich FET presents steady field effect. When V_G is -30V, the NdNc sandwich FET's hole mobility in the saturation region is $0.05cm^2/V.s$ and the threshold voltage is -12V. Table 2 lists the performance parameters of the FET sandwiched new organic semiconductor, in which case, the mobility is under the constraint that V_G equals to -30V.

Table 2

Semiconductor 4	Semiconductor 6	Hole mobility $cm^2/V.s$
CuPc	$LaPc_2$	0.02
CuPc	$CePc_2$	0.017
CuPc	$PrPc_2$	0.025
CuPc	$NdPc_2$	0.015
CuPc	$SmPc_2$	0.01
CuPc	$EuPc_2$	0.03
CuPc	$GdPc_2$	0.025
CuPc	$TbPc_2$	0.009
CuPc	$DyPc_2$	0.02
CuPc	$HoPc_2$	0.01
CuPc	$ErPc_2$	0.05
CuPc	$TmPc_2$	0.03
CuPc	$YbPc_2$	0.03
CuPc	$LuPc_2$	0.07
CuPc	YPc_2	0.05
CuPc	$ZrPc_2$	0.06
CuPc	$HfPc_2$	0.02
CuPc	$SnPc_2$	0.007
CuPc	H_2Nc	0.01
CuPc	CoNc	0.08
CuPc	CuNc	0.02
CuPc	ZnNc	0.05
CuPc	NiNc	0.02

Example 3:

$F_{16}CuPc$ and $F_{16}ZnPc$ used in the present experiment are commercial products,

which have been sublimated and purified before being used.

On the 7059 glass substrate or the flexible plastic substrate 1, a film layer of metal Ta with about 200 nm in thickness was plated by using the radio frequency (RF) magnetism controlled sputtering method and shaped into the gate electrode 2 by the photolithography method. On the gate electrode, a film layer of Ta_2O_5 with a thickness of about 100 nm was reactively sputterred as the gate insulation layer 3 by the direct current (DC) magnetism controlled sputtering method. Then depositing $F_{16}CuPc$ using the molecular vapor phase deposition method to prepare the active layer 4 having a thickness of about 20 nm. Subsequently, using Au to prepare the source electrode and the drain electrode 5 with a thickness of about 50 nm by the photolithography technology. Finally, depositing $F_{16}ZnPc$ using the molecular vapor phase deposition method to form the active layer 6 having a thickness of about 30nm. The electron mobility of the sandwich field effect devices is $0.02cm^2/V.s$ in the saturation region. The electron mobility of the $F_{16}CuPc$ and $F_{16}ZnPc$ sandwich FET is $0.016cm^2/V.s$ in the saturation region.

The present invention has been described by way of the above examples. The present invention is not limited to the modes described in the respective examples but naturally includes various other modes according to the principle of the present invention. In general, the sandwich FET according to the present invention can be processed to the elements of the 2D and 3D integrated devices. These integrated devices can be applied in flexible IC, the active matrix display and the like. The FET according to the present invention can be processed at low temperature. Besides the traditional photoetching, many methods such as mimeograph, printing and the like can be used to prepare the bipolar type FET of the present invention.